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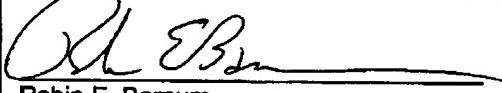
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of
Joseph R. Zbiciak
Serial No.: 09/703,034
Filed: October 31, 2000
For: Microprocessor With Rounding Dot Product Instruction

TI-30553
Art Unit: 2124
Examiner: Chat C. Do
Conf. No.: 8913

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Applicant: Zbiciak

Art Unit: 2124

Serial No.: 09/703,034

Examiner: Chat C. Do

Filed: October 31, 2000

Docket: TI-30553

For: MICROPROCESSOR WITH ROUNDING DOT PRODUCT INSTRUCTION

Appeal Brief under 37 C.F.R. §41.37

Board of Patent Appeals and
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Robin E. Barnum

Dear Sir:

This is Appellant's Appeal Brief filed pursuant to 37 C.F.R. §41.37 and the Notice of Appeal filed June 15, 2005 and further in response to the NOTIFICATION OF NON-COMPLIANT APPEAL BREIF of December 1, 2005.

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Real Party in Interest

The real party in interest in this application is Texas Instruments Incorporated, a corporation of Delaware with its principle place of business in Dallas, Texas. An assignment to Texas Instruments Incorporated is recorded at reel 011536 and frames 0374 and 0375.

Related Appeals and Interferences

There are no appeals or interferences related to this appeal in this application.

Status of the Claims

Claims 1, 4, 5, 9 to 11, 13 and 17 are rejected and subject to this appeal. No claims are allowed.

Status of Amendments Filed After Final Rejection

No amendments to the claims were proposed following the FINAL REJECTION of February 23, 2005.

Summary of Claimed Subject Matter

This invention is a method of performing a dot product operation with rounding and shifting in a microprocessor in response to a single rounding dot product instruction (claim 1, page 16, lines 6 to page 17, line 11, Figure 3A) and an apparatus to practice the method (claim 13, page 4, lines 19 to 27).

The method (claim 1) fetches a first pair of elements and a second pair of elements (300, 301). The method forms a first product of the first pair of elements (310) and a second product of the second pair of elements (311). The method combines the first product with the second product to form a combined product (320) in an arithmetic circuit (420, 520, 620). The arithmetic circuit is also used to round the combined product (330) to form an

intermediate result via a carry input to a mid-position (MRND) receiving a rounding value. The method right shifts the intermediate result a selected amount to form a final result (340).

The method (claim 4, page 30, lines 4 to 7) preferably has a rounding value is 2^n and a selected shift amount of $n+1$. This fixed value n is preferably 15 (claim 5, page 18, lines 13 to 15).

The method may form the first and second products by treating a first element of the first pair of elements as a signed number value and the second element as an unsigned number value (claim 9, page 18, lines 2 to 5).

The combining step may be subtracting the second product from the first product (claim 10, lines 9 to 11) or adding the first and second products (claim 11, page 18, lines 7 to 9).

The shifting step sign extends the intermediate result (claim 16, page 18, lines 22 to 26).

The apparatus (claim 13) is a digital system having a microprocessor (page 7, lines 3 to 6, Figure 1) operable to execute a rounding dot product instruction (Figure 3B). This digital system includes storage circuitry for holding pairs of elements (page 7, lines 24 to 25, 20a, page 8, lines 4 to 5, 20b), a multiply circuit (410, 411 of Figure 4, MPY0 and MPY1 of Figures 5 and 6), an arithmetic circuit (420, 520, 620) and a shifter (440, 540, QSH- of Figure 6). The multiply circuit receives a first number of pairs of elements from the storage circuitry in a plurality of multipliers equal to the first number of pairs of elements (page 20, lines 19 to 24, page 24, lines 9 to 10, page 25, lines 20 to 24). The arithmetic circuit receives the plurality of products from the plurality of multipliers (page 22, lines 4 to 20, page 24, line 22 to page 25, line 2, page 26, lines 15 to 26) and a mid-position carry input for mid-position rounding (page 22, lines 21 to 28, page 25, lines 3 to 10, page 25, line 27 to page 27, line

5). The shifter shifts the output of the arithmetic circuit a selected amount (page 23, lines 8 to 10, page 25, lines 11 to 14).

The shifter (claim 17) right shifts by the selected amount and sign extends the output of the arithmetic circuit (page 22, lines 26 to 28, page 25, lines 8 to 10, page 27, lines 3 to 5).

This application includes no "means plus function" or "step plus function" claims.

Grounds for Rejection to be Reviewed on Appeal

Claims 1, 4, 5, 10, 11, 13, 16 and 17 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Pitsianis et al U.S. Patent Application Publication No. U.S. 2003/0088601 and Adelman et al U.S. Patent No. 5,666,300. The FINAL REJECTION states at page 2, line 23 to page 3, line 6 that Pitsianis et al discloses:

"rounding (627) the combined product to form an intermediate result via an arithmetic circuit (627) having a first input receiving said first product, a second input receiving said second product and a carry input to a mid-position receiving said rounding value to form the intermediate result (Figure 2B with rounding architecture and col. 3 0049-0054 wherein the carry-input is a rounding factor according to conventional rounding architecture as ROUND, TRUNC, CEIL, or FLOOR and in Figure 3B the shifting/dividing is done prior rounding)"

The RESPONSE TO ARGUMENTS of the FINAL REJECTION at page 5, line 15 to page 6, line 3 states:

"The examiner respectfully submits that Figure 2B discloses different rounding modes including truncating, ceiling, flooring, and rounding mode. An instant case of an inherent and well known technique in the art for ceiling mode is to add a factor called carrying factor or rounding factor (either 0 or 1) to the rounding number (e.g. 33.6 will be 34 wherein 1 carry factor will be added to 33 for round up) to correctly round toward positive number. In addition, the MPYCX instruction in Figure 2B is rounding upper 16-bit portion of

30-bit in line 3 of table. From all above, there must be a carry input or carrying factor of certain rounding modes added to the last bit of upper 16-bit portion of the 30-bit result number."

Regarding claims 16 and 17, the FINAL REJECTION states at page 4, lines 6 to 11:

Re claim 16, Pitsianis et al. further disclose in Figures 3B and 6 the step of shifting further includes sign extending the intermediate result (Figure 18, selecting only 30-15 out of 30 bits).

Re claim 17, Pitsianis et al. further disclose in Figures 3B and 6 the shifter right shifts the output of the arithmetic circuit the selected amount and sign extends the output of the arithmetic circuit (Figure 18, selecting only 30-15 out of 30 bits).

Accordingly, the Examiner submits that claims 1, 4, 5, 10, 11, 13, 16 and 17 are made obvious by the combination of Pitsianis et al and Adelman et al.

Claim 9 was rejected under 35 U.S.C. 103(a) as made obvious by the combination of Pitsianis et al U.S. Patent Application Publication No. U.S. 2003/0088601, Adelman et al U.S. Patent No. 5,666,300 and Slavenburg et al U.S. Patent No. 5,963,744. The FINAL REJECTION states at page 4, line 15 to page 5, line 8:

Pitsianis et al. in view of Adelman et al. do not disclose the steps of forming the first product and forming the second product treats a one of the first pair of elements as a signed number value and treats another one of the first pair of elements as an unsigned number value. However, Slavenburg et al. disclose in Figure 18 a dot product wherein the steps of forming the first product (e.g. first element of rsrc2 and rsrc1) and forming the second product (e.g. second element of rsrc2 and rsrc1) treats a one of the first pair of elements as a signed number value (rsrc2) and treats another one of the first pair of elements as an unsigned number value (rsrc1). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the steps of forming the first product and forming

the second product treats a one of the first pair of elements as a signed number value and treats another one of the first pair of elements as an unsigned number value as seen in Slavenburg et al.'s invention into the combined invention of Pitsianis et al. in view of Adelman et al. because it would enable to increase the flexibility of the system by handling multiple formatted operand registers (col. 2 lines 65-67).

Accordingly, the Examiner submits that claim 9 is made obvious by the combination of Pitsianis et al, Adelman et al and Slavenburg.

Arguments

Claims 1, 4, 5, 10, 11, 13, 16 and 17 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Pitsianis et al U.S. Patent Application Publication No. U.S. 2003/0088601 and Adelman et al U.S. Patent No. 5,666,300.

Claims 1 and 13 recite subject matter not made obvious by the combination of Pitsianis et al and Adelman et al. Claim 1 recites "combining the first product with the second product to form a combined product and rounding the combined product to form an intermediate result via an arithmetic circuit." Claim 13 similarly recites "an arithmetic circuit having a plurality of inputs each connected to receive a corresponding one of the plurality of products from the plurality of multipliers and a mid-position carry input for mid-position rounding responsive to the rounding dot product instruction." The FINAL REJECTION states at page 2, line 23 to page 3, line 6 that Pitsianis et al discloses:

"rounding (627) the combined product to form an intermediate result via an arithmetic circuit (627) having a first input receiving said first product, a second input receiving said second product and a carry input to a mid-position receiving said rounding value to form the intermediate result (Figure 2B with rounding architecture and col. 3 0049-0054 wherein the carry-input is a rounding factor according to conventional rounding architecture as ROUND, TRUNC, CEIL, or FLOOR and in Figure 3B the shifting/dividing is done prior rounding)"

The RESPONSE TO ARGUMENTS of the FINAL REJECTION at page 5, line 15 to page 6, line 3 states:

"The examiner respectfully submits that Figure 2B discloses different rounding modes including truncating, ceiling, flooring, and rounding mode. An instant case of an inherent and well known technique in the art for ceiling mode is to add a factor called carrying factor or rounding factor (either 0 or 1) to the rounding number (e.g. 33.6 will be 34 wherein 1 carry factor will be added to 33 for round up) to correctly

round toward positive number. In addition, the MPYCX instruction in Figure 2B is rounding upper 16-bit portion of 30-bit in line 3 of table. From all above, there must be a carry input or carrying factor of certain rounding modes added to the last bit of upper 16-bit portion of the 30-bit result number."

The Applicants do not dispute that Pitsianis et al discloses rounding. The Applicants urge that the manner of rounding recited in claims 1 and 13 is unobvious over the manner of rounding disclosed in Pitsianis et al. Both claims 1 and 13 require the rounding to take place during the arithmetic combining of the two products. Claim 1 recites the rounding takes place "via an arithmetic circuit" during the combining of the first and second products. Claim 13 recites "an arithmetic circuit...for mid-position rounding." Pitsianis et al discloses at paragraph [0054]:

"The selection of the bits and rounding occurs in selection and rounder circuit 627."

and at paragraph [0055]:

"The results from adder 723 and subtractor 725 still need to be selected and rounded in selection and rounder circuit 727 and the final rounded results stored in the target register 729 in the CRF."

Pitsianis et al thus teaches that rounding takes place in selection and rounder circuit 627 or in selection and rounder circuit 727. The FINAL REJECTION cites adder 625 as making obvious the combining step of claim 1 and the adder circuit of claim 13. Thus the FINAL REJECTION states and Pitsianis et al teaches that the rounding takes place in a different method step (claim 1) or in a different structure (claim 13) than recited in the claims. Accordingly, claims 1 and 13 are not made obvious by the combination of Pitsianis et al and Adelman et al.

Claims 1 and 13 recite further subject matter not made obvious by the combination of Pitsianis et al and Adelman et al. Claim 1 recites "a carry input to a mid-position receiving said rounding value to form the intermediate result." Claim 13 similarly recites "a mid-position carry input for mid-position rounding responsive to the rounding dot product instruction." Pitsianis et al fails to teach or make obvious the recited mid-position carry input. In this invention, the bits to be output are selected by shifting following the rounding. The use of a mid-position carry input during the arithmetic combining of products is useful in this rounding. The normal manner of rounding using an arithmetic operation is to provide a carry input into the least significant bit of the arithmetic logic unit. Since this invention will eventually discard the least significant bits of the arithmetic combination, using this prior art technique would result in additional processing time for the carry ripple of the rounding input through those bits that will be discarded. Claim 1 recites "a carry input to a mid-position receiving said rounding value to form the intermediate result." Claim 13 similarly recites "a mid-position carry input for mid-position rounding responsive to the rounding dot product instruction." Such a mid-position carry input causes the carry input to change only those bits that will be retained after the shifting. While the FINAL REJECTION states that this is disclosed in Pitsianis et al, in fact neither subtractor 623, adder 625 of Figure 6 nor adder 723, subtractor 725 of Figure 7 illustrate the "mid-position carry input" recited in claims 1 and 13. The cited test of paragraphs [0049] to [0054] disclose rounding modes without disclosing the recited "mid-position carry input." Further, Pitsianis et al includes no mention of "mid-position" or of "carry input." Accordingly, claims 1 and 13 are not made obvious by the combination of Pitsianis et al and Adelman et al.

Claims 16 and 17 recite subject matter not made obvious by the combination of Pitsianis et al and Adelman et al. Claim 16 recites "the step of shifting further includes sign extending the intermediate result." Claim 17 recites the shifter "sign extends the output of the arithmetic circuit." The FINAL REJECTION cites rounder circuit 627 illustrated in Figure 6 of Pitsianis et al as disclosing this element in "selecting only 30-15 out of 32 bits." The FINAL REJECTION further states it would be obvious to substitute the shifter illustrated in Figure 2 of Adelman et al for the selector of Pitsianis et al. The RESPONSE TO ARGUMENTS of the FINAL REJECTION at page 6, lines 6 to 10 states:

"The examiner respectfully submits that Figure 18 clearly shows a sign of operand must maintain throughout the operations in order to provide the correct result. In addition, the shifting and selecting process is selecting upper 16-bit portion including the most significant bit (MSB) as signed bit. Therefore, the cited reference of Pitsianis et al. inherently disclose an 'sign extending' in operations."

The Applicant respectfully submits this is in error. "Sign extending" and "sign extend" are terms known in the art. A signed number has a most significant bit indicating the sign. A "0" indicates a positive number while a "1" indicates a negative number. Sign extension duplicates this most significant bit to maintain the sign indication following the shift operation. Pitsianis et al include no such disclosure. In fact, Pitsianis et al includes no teaching of signed numbers and therefore cannot teach the claimed sign extension. The additional teaching of Pitsianis et al regarding Figure 18 concerns addition for some inputs to adders 1823 and 1825 and subtraction for other inputs. Adelman et al does disclose "sign extension" in conjunction with accumulator registers 83 and 84 where 8-bit registers A2 and B2 store a sign extension. Neither Pitsianis et al nor Adelman et al

teach sign extension during shifting as recited in claim 1 or sign extension by a shifter as recited in claim 13. Accordingly, claims 16 and 17 are allowable over the combination of Pitsianis et al and Adelman et al.

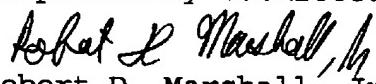
Claims 4, 5, 10 and 11 are allowable by dependence upon respective allowable base claims 1 and 13.

Claim 9 was rejected under 35 U.S.C. 103(a) as made obvious by the combination of Pitsianis et al U.S. Patent Application Publication No. U.S. 2003/0088601, Adelman et al U.S. Patent No. 5,666,300 and Slavenburg et al U.S. Patent No. 5,963,744.

Claim 9 is allowable by dependence upon allowable base claim 1.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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CLAIMS APPENDIX

1 1. A method of performing a dot product operation with
2 rounding and shifting in a microprocessor in response to a single
3 rounding dot product instruction, the method comprising the steps
4 of:

5 fetching a first pair of elements and a second pair of
6 elements;

7 forming a first product of the first pair of elements and a
8 second product of the second pair of elements;

9 combining the first product with the second product to form a
10 combined product and rounding the combined product to form an
11 intermediate result via an arithmetic circuit having a first input
12 receiving said first product, a second input receiving said second
13 product and a carry input to a mid-position receiving said rounding
14 value to form the intermediate result; and

15 right shifting the intermediate result a selected amount to
16 form a final result.

1 4. The method of Claim 1, wherein the rounding value is 2^n
2 and the selected shift amount is $n+1$.

1 5. The method of Claim 4, wherein n has a fixed value of
2 fifteen.

1 9. The method of Claim 1, wherein the steps of forming the
2 first product and forming the second product treats a one of the
3 first pair of elements as a signed number value and treats another
4 one of the first pair of elements as an unsigned number value.

1 10. The method of Claim 1, wherein the step of combining
2 comprises subtracting the product of second pair of elements from
3 the product of first pair of elements.

1 11. The method of Claim 1, wherein the step of combining
2 comprises adding the product of second pair of elements to the
3 product of first pair of elements.

1 13. A digital system having a microprocessor operable to
2 execute a rounding dot product instruction, wherein the
3 microprocessor comprises:

4 storage circuitry for holding pairs of elements;
5 a multiply circuit connected to receive a first number of
6 pairs of elements from the storage circuitry in a first execution
7 phase of the microprocessor responsive to the dot product
8 instruction, the multiply circuit comprising a plurality of
9 multipliers equal to the first number of pairs of elements;
10 an arithmetic circuit having a plurality of inputs each
11 connected to receive a corresponding one of the plurality of
12 products from the plurality of multipliers and a mid-position carry
13 input for mid-position rounding responsive to the rounding dot
14 product instruction; and
15 a shifter connected to receive an output of the arithmetic
16 circuit, the shifter operable to shift a selected amount in
17 response to the rounding dot product instructions.

1 16. The method of Claim 1, wherein:
2 the step of shifting further includes sign extending the
3 intermediate result.

1 17. The digital system of Claim 13, wherein:
2 the shifter right shifts the output of the arithmetic circuit
3 by the selected amount and sign extends the output of the
4 arithmetic circuit.